R860

Wide-range RF Tuner

For SDR Applications

General Description

The R860 wide-range RF tuner achieves low power consumption in a small form factor with very high RF performance for Software Defined Radio (SDR) applications. With innovative AccuTune™ and TrueRF™ techniques, the R860 provides superior performance for RF sensitivity, linearity, adjacent channel immunity and image rejection. It has an integrated smart power detector to optimize RF performance in different input power scenarios and give exceptional spurious-free dynamic range.

The R860 is a highly integrated silicon tuner that includes a low noise amplifier (LNA), RF mixer, fractional PLL, variable gain amplifier (VGA), voltage regulator and tracking filter. It eliminates the need for external SAW filters, external LNA, balun transformer and low drop-out (LDO) regulator. With an advanced LNA architecture, the R860 offers the lowest cost and highest performance for SDR applications. The on-chip LDO, high performance LNA and small package size enable a perfect solution for SDR applications.

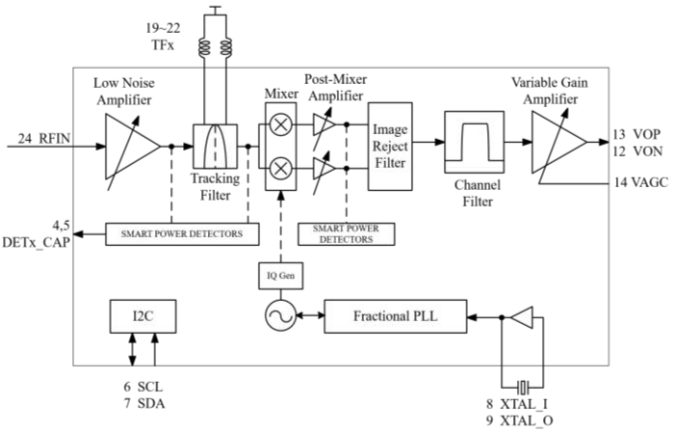
With proprietary “Green RF” techniques, the R860 achieves both the highest performance and the lowest power consumption which fits perfectly with worldwide trends. The R860 comes in a small thin 4x4mm 24-lead QFN RoHS compliant package.

Features

- Frequency range: 24MHz~ 1766MHz
- Typical gain rage: 96dB
- Typical Noise Figure: 4dB
- High Linearity IIP3: -4dBm (Typical at LNA Max Gain)
- Compliant with EN-55020, EN55013 and FCC
- 2-wire I^2C interface
- Single 3.3V DC supply with current <190mA
- Halogen-free / RoHS 2.0 / Reach Annex 14 & 17

Applications

- Terrestrial and cable TV / Set Top Box
- Radio Spectrum Monitoring
- FM and AM Radio Reception
- Amateur Radio
- ADS-B
- Emergency and Public Service Signals



1. Absolute Maximum Ratings

Parameters	Symbol	Min	Typical	Max	Units
Supply Voltage to GND	V_{cc}	-0.3		3.6	V
I2C input voltage (SCL, SDA) to GND		-0.3		3.6	V
AGC control for VGA to GND	IF_AGC	-0.3		3.6	V
Xtal_I / Xtal_O / CLK_Out		-0.3		3.6	V
RF input to GND	RFin	-0.3		2.2	V
Det1 / Det2 / CP		-0.3		2.6	V
Voltage on All Other Pins		0.7		2.6	V
Operating Temperature	T_{op}	-20		85	°C
Storage Temperature	T_{STG}	-65		150	°C
Maximum Junction Temperature	T_J		125		°C
Reflow Soldering – Peak Temperature				260	°C
– Time at Peak Temperature				30	s

2. Electrical Parameters

Table 2-1 DC Parameters

Parameters	Condition	Min	Typical	Max	Units
VCC Input voltage		3.0	3.3	3.6	V
Sleeping Mode Current	Loop-through OFF		11		mA
Standby Mode Current	Loop-through ON		64		mA
Total Current Consumption	After Programming		190	210	mA

Notes:

1. All DC currents are measured under 3.3V and 27 °C

Table 2-2 AC Parameters

Parameters	Condition	Min	Typical	Max	Units
Input Return Loss[1]	S11		-10		dB
Tuning Frequency Range		24		1766	MHz
Gain Range			96		dB
Noise Figure	@ Max Gain		4		dB
IIP3[2]	LNA Max Gain		-4		dBm
	LNA Min Gain		+35		dBm
Image Rejection			65		dBc
Phase Noise[3]	1KHz		-91		dBc
	10KHz		-97		dBc
	100KHz		-115		dBc
CSO	110 Channel at 75dBμV		-67		dBc
CTB			-65		dBc
Multiple Crystal Frequency Spurious	Refer to RF-In		-120		dBm
RF in to Loop through gain [1]			0		dB
Loop-through Return Loss[1]			-13		dB
Sensitivity	FFT:8k,QPSK,CR:1/2		-97.5		dBm
	FFT:8k,16QAM,CR:1/2		-91.5		dBm
	FFT:8k,64QAM,CR:3/4		-81.5		dBm
Adjacent Channel Rejection	FFT:8k,64QAM,CR:7/8		-79.5		dBm
	Analog Interference on DVB-T Signal		-47		dBc
Maximum Input Power	FFT:8k,64QAM,CR:7/8		+10		dBm
IF Output	Swing		1	2	V_{p-p}
	Impedence	Differential 2kΩ//5pF			
PLL Locking time				5	ms

Notes:

1. 75ohm system
2. IIP3 is measured with two tones at 900 MHz and 900.5 MHz
3. Phase noise is measured at 200MHz

3. Pin Assignments And Descriptions

Figure 3-1 Pin Assignments (note: E-Pad is GND)

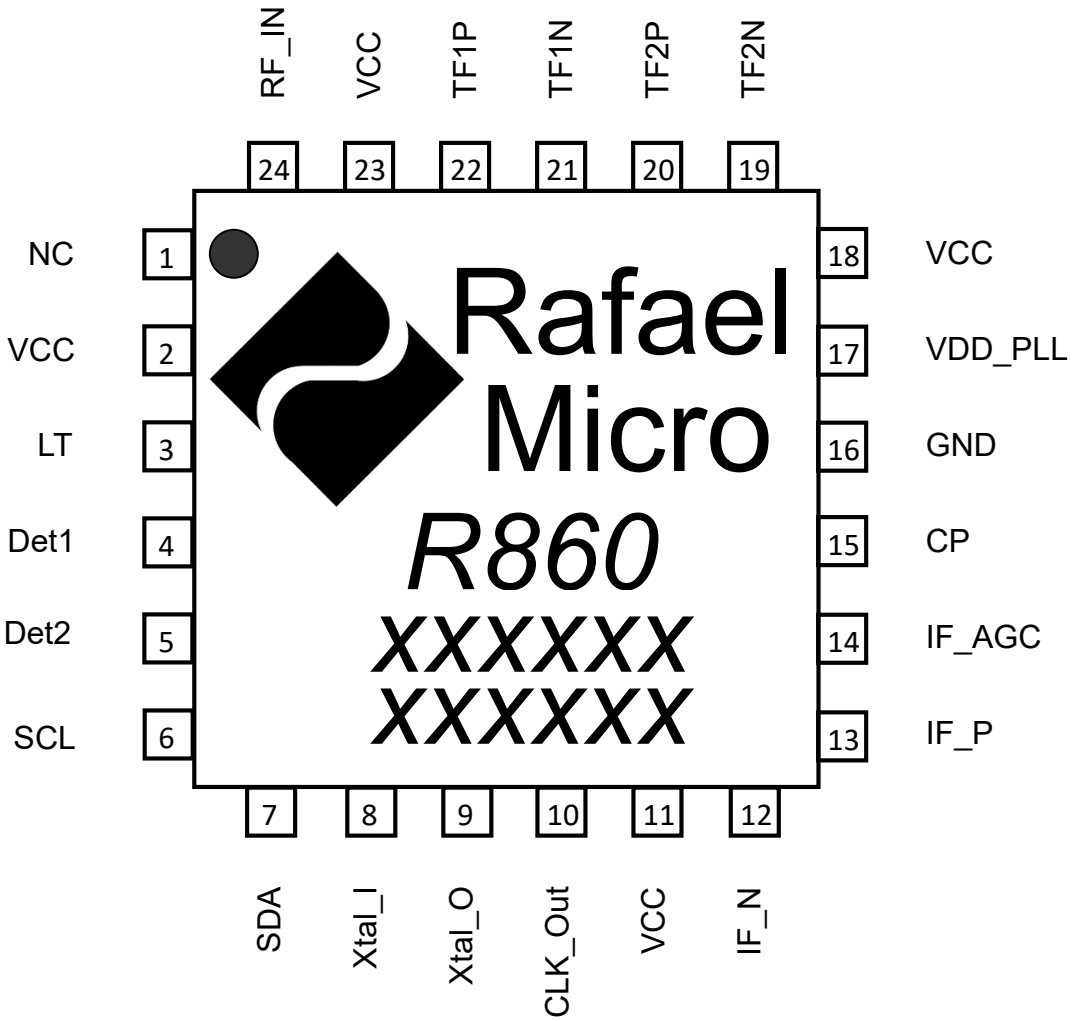


Table 3-1 Pin Descriptions

Pin Number	Symbol	Description
24	RF_IN	RF Input to internal LNA. This pin has a DC voltage, so a capacitor needs to be connected in series between it and the external antenna or external ESD protection such as BAV99 for DC isolation.
1	NC	No Connect
2,11, 18,23	VCC	3.3VDC supply voltage. Decoupling capacitors to the ground should be placed as close as possible to the VCC pins.
3	LT	Loop-through output. This pin has a DC voltage, so a capacitor needs to be connected in series between it and the next stage RF input or external ESD protection such as BAV99 for DC isolation.
4,5	Det1, Det2	Det1: External capacitor connection for the power detector controlling LNA gain. Det2: External capacitor connection for the power detector controlling post-mixer amplifier gain The power detector is a key block of the automatic gain control (AGC). It converts the AC signal from the gain stages into a DC level through an external capacitor, which is then processed by the digital circuitry to provide feedback control of the circuit gain
6,7	SCL, SDA	SCL: I2C bus, clock input. SDA: I2C bus, serial data input/ output. The I²C interface supports a typical speed of 100KHz, with a maximum speed up to 1MHz.
8,9	Xtal_I, Xtal_O	Crystal oscillator input and output
10	CLK_Out	Clock output for sharing the crystal oscillator signal. A capacitor is suggested to be connected in series between it and the next stage.
12,13	IF_N, IF_P	IF outputs. The IF is a low-IF system with a frequency range of 0.5MHz to 10MHz. Since the output has a DC bias of VCC/2, it is recommended to AC-couple the signal to the subsequent IC (e.g., a demodulator) through a series capacitor

14	IF_AGC	IF automatic gain control input. The IF_AGC input is voltage-controlled; a higher input voltage results in a higher corresponding VGA gain. Within the input range of 0.6 V to 2.5 V, the controllable VGA gain range is approximately 47 dB
15	CP	PLL charge pump. It provide $\pm I_{cp}$ to the external loop filter, in turn, drives the VCO. Additionally, the ground connection of the external loop filter from CP pin must be connected to the adjacent ground pin (Pin 16) in PCB layout
16	GND	Ground for PLL.
17	VDD_PLL	PLL 2V supply output decoupling. The VDD_PLL pin is the output of an internal LDO regulator. It requires an external decoupling capacitor connected to the adjacent ground pin (Pin 16) in PCB layout. For optimal performance, this decoupling capacitor should be close to the VDD_PLL.
19,20,21,22	TF2N, TF2P TF1N, TF1P	Tracking filters. The differential tracking filter in broadband RF applications provides selectivity and effectively handles harmonic rejection, requiring specific settings for different frequencies. This architecture requires two external inductors: one connected between TF1N and TF1P, and the other between TF2N and TF2P. For optimal performance, the external inductors should be placed as close as possible to the TF pins (Pins 19–22).
0	GND	Exposed pad (E-pad)

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4. Performance Characteristics

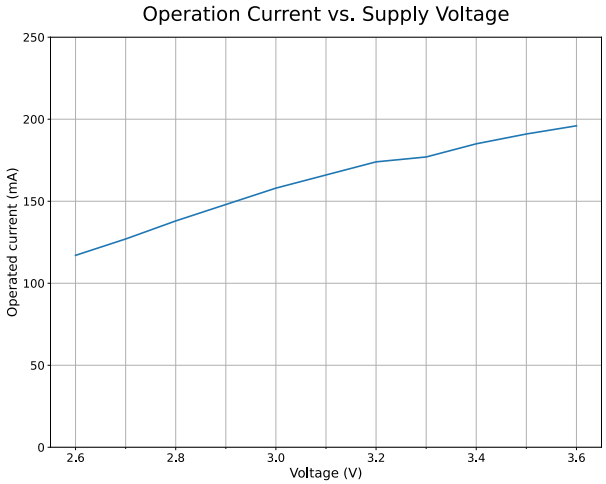


Fig 4.1 Operation current vs Supply Voltage

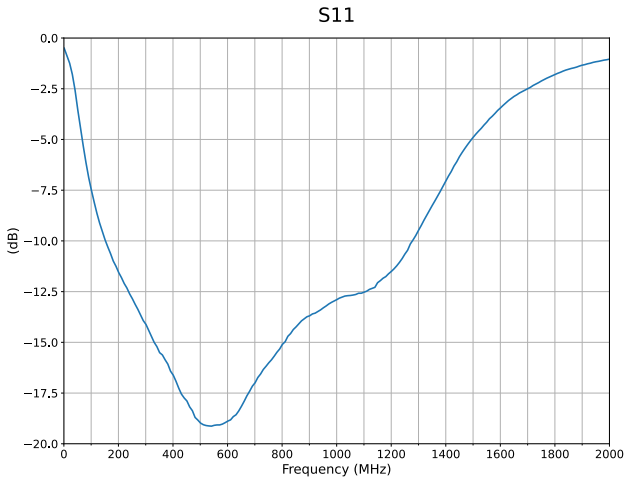


Fig. 4.2 Return Loss (S11) at maximum LNA gain under a 75 Ω load measured on the EVB shown in Section 7.

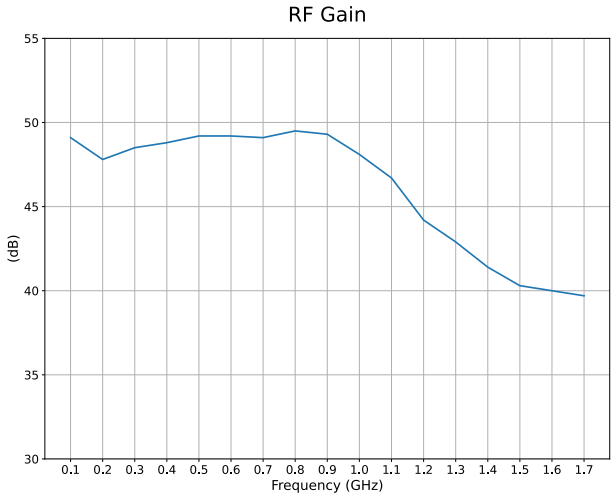


Fig. 4.3 RF Gain Range (excluding IF VGA gain range)

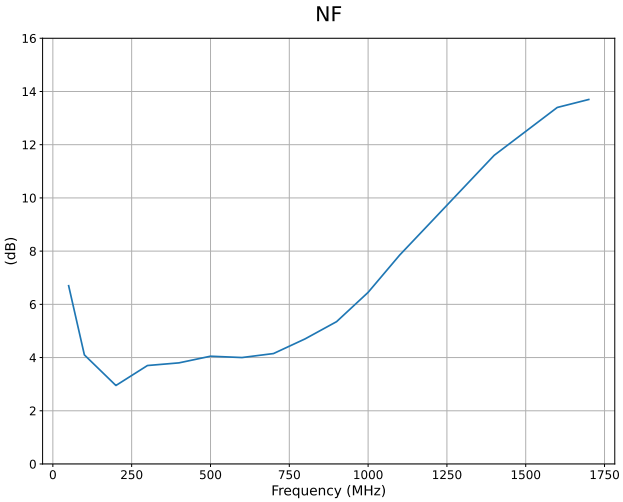


Fig. 4.4 Noise Figure (NF) vs Frequency measured on the EVB shown in Section 7.

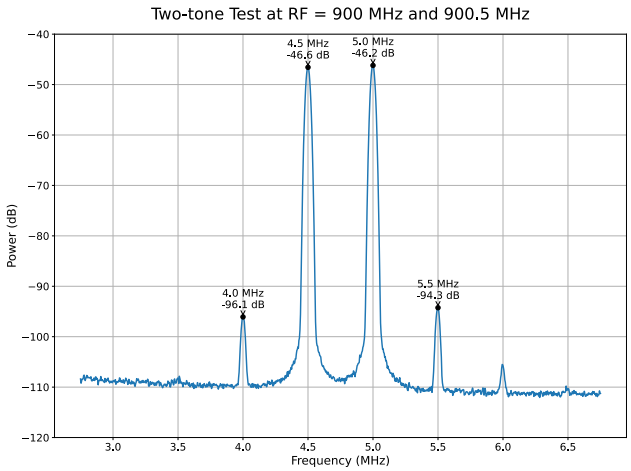


Fig. 4.5 Two-tone test at RF= 900 MHz and 900.5 MHz, measured at the IF outputs (pin 12 & pin 13). The ΔIM3 is approximately 48 dBc under an RF input power of –28 dBm, indicating an IIP3 of –28 + 48/2 = –4 dBm.

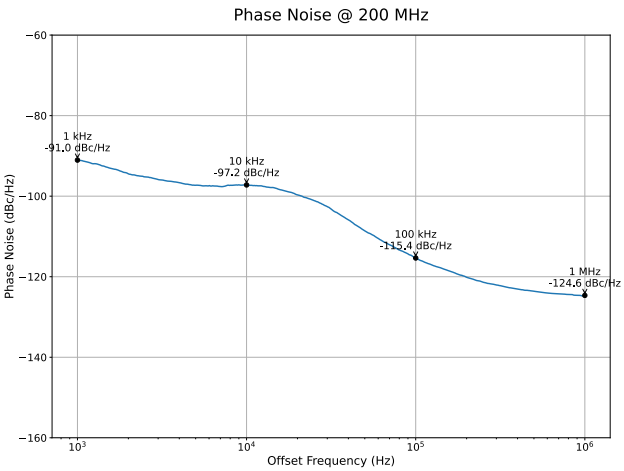


Fig. 4.6 Phase noise measured at 200MHz.

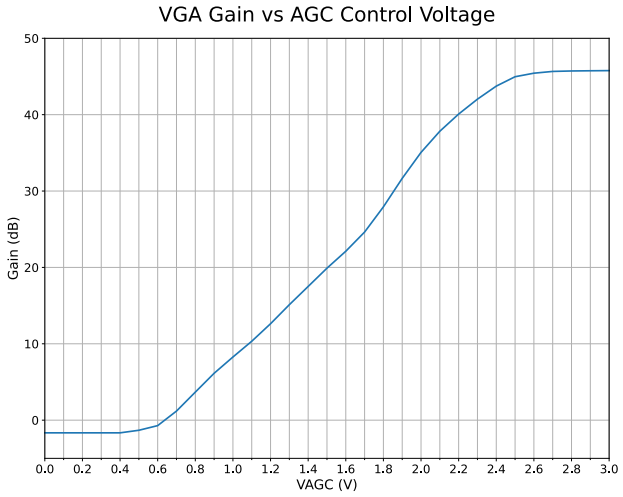


Fig. 4.7 The VGA can be externally controlled by the demodulator through the IF_AGC (pin 14) voltage ranging from 0.6 V to 2.5 V, providing a wide gain range from -1.5 dB to +45.5 dB.

5. Theory of Operation

RF Input

For applications covering a wide frequency range (40 MHz to 1.7 GHz), avoid placing any matching inductor at the RF input (Pin 24). Since the LNA self-bias at the RF input is around 1.74 V, a DC-blocking capacitor, 470pF, is recommended in front of the RF input.

Crystal Requirements

For compact product designs, a low-profile SMD crystal is recommended. The default system frequency is 16 MHz, and the verified component part number is X3S016000BG1HA-HZ. For alternative crystal frequencies (e.g., 12, 20, 20.48, 24, 27, 28.8, or 32 MHz), please contact Rafael Micro Applications Engineering for recommendations.

Table 5-1 Crystal Parameters

Parameter	Min	Typical	Max	Units
Frequency		16		MHz
ESR			50	Ω
Frequency accuracy		± 30	± 50	ppm
Load Capacitor (CL)		12		pF

For the default 16 MHz crystal on Rafael Micro's EVB, parallel load capacitors of C1 = C2 = 19 pF are recommended (see Figure 5-1). The effective load capacitance is calculated as:

$$C_L = \frac{C1 \cdot C2}{C1 + C2} + C_{stray}$$

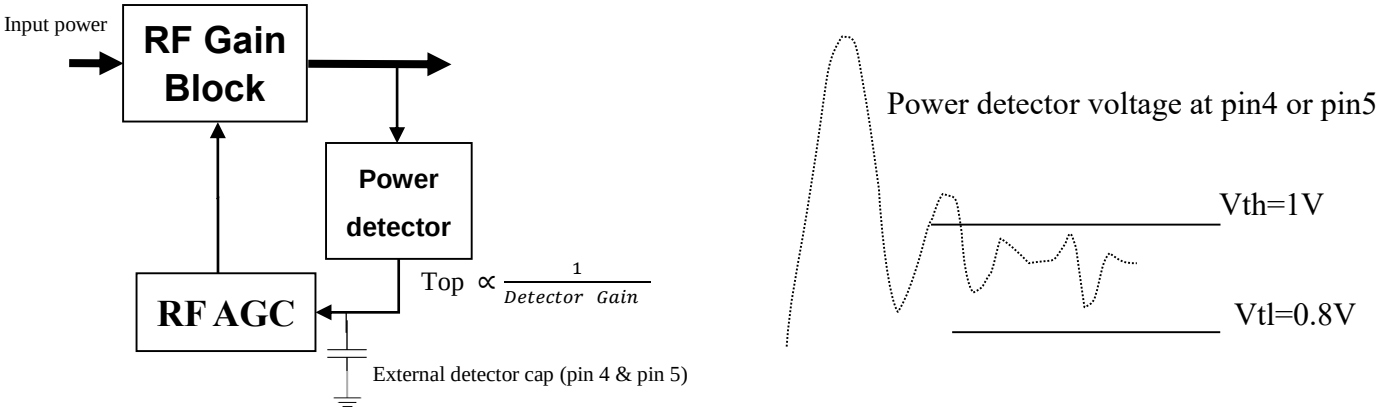
where C1 = C2 and Cstray ≈ 2.5 pF, accounting for parasitic capacitance from PCB traces, crystal pins, and surrounding components. This configuration provides the required load capacitance for a 16 MHz crystal.

For cost-sensitive designs, R860 can share its crystal with a demodulator or baseband IC to minimize external components. The clock output on Pin10 provides a triangle wave with a typical swing of > 2.0 Vp-p (assuming load < 2 pF). This output can be enabled or disabled through Register 24 via the I²C control interface.

RF Automatic Gain Control (AGC)

The R860 integrates an **RF AGC** to maintain optimal SNR while minimizing distortion. When the RF input power increases, the internal power detector automatically reduces the RF gain; when the input power decreases, it increases the gain to ensure the best IF output quality. The RF AGC operation is illustrated in Figure 5-2, where the RF_AGC adjusts the gain to keep the power detector voltage within the target range [Vth, Vtl]. If the voltage deviates from this range, the RF_AGC instructs the RF gain block to readjust the gain to bring it back within this range.

Figure 5-2 Closed-loop of RF AGC



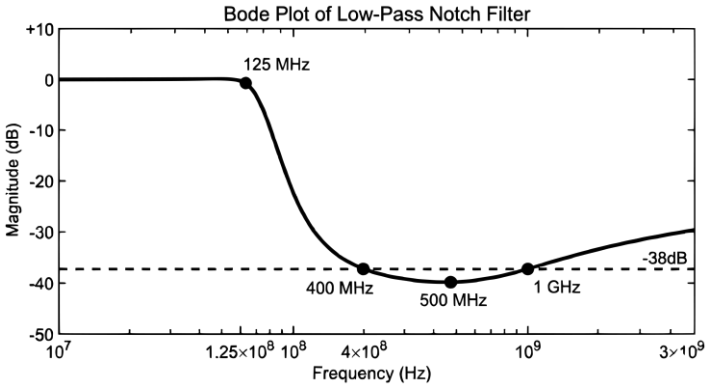
Tracking Filter

Tracking Filter Architecture R860 integrates a differential tracking filter utilizing a low-pass notch architecture designed to provide high selectivity and effective harmonic rejection for the RF front-end.

Harmonic Rejection Example Figure 5-3 illustrates a typical frequency response where the low-pass corner frequency is set to 125 MHz. In this configuration, the notch frequency range (400 MHz to 1 GHz) provides approximately 38 dBc of attenuation for the 3rd (375 MHz), 5th (625 MHz), and 7th (875 MHz) harmonics of the desired 125 MHz signal.

Configuration and Control For TV and Set-Top Box (STB) applications, this differential tracking filter requires external 150nH inductors connected to the TF pins (Pins 19–22).

Figure 5-3 Bode Plot of LPF Notch Fitler



The filter characteristics are fully register-programmable:

Corner Frequency: Adjusted via TF_LP[3:0] (R27[3:0]).

Notch Frequency: Adjusted via TF_NCH[3:0] (R27[7:4]).

Bypass Mode: To bypass the tracking filter, set RFMUX[1:0] (R26[7:6]) to 1.

VCO and LO Formula

The PLL divider ratio, Ndiv, is defined as:

$$Ndiv = (Nint + Nfra) \cdot 2$$

Where:

- Nint (Integer Part) = 4 · N_I2C + S_I2C + 13
- Nfra (Fractional Part) = SDM_IN[15] · 2^{-1} + SDM_IN[14] · 2^{-2} + ⋯ + SDM_IN[1] · 2^{-15} + SDM_IN[0] · 2^{-16}.

Register Configuration

The integer part (Nint) is configured via N_I2C[5:0] (R20[5:0]) and S_I2C[1:0] (R20[7:6]). The fractional part (Nfra) is determined by SDM_IN[15:0], located in registers R21[7:0] and R22[7:0].

Frequency Calculation

The VCO frequency is derived from the 16 MHz reference clock:

$$VCO = 16\ MHz \cdot Ndiv$$

The LO frequency is obtained by dividing the VCO frequency by the SEL_DIV[2:0] ratio (set in R16[7:5]):

$$LO = VCO / SEL\_DIV[2:0]$$

Example Calculation Target: LO = 605 MHz

1. Select Divider: Set SEL_DIV = 4.
2. Calculate Required VCO = 605 MHz · 4 = 2420 MHz.
3. Calculate Ndiv: N_div = 2420 MHz / 16 MHz = 151.25.
4. Determine Register Parameters:
    - From N_div = (N_int + N_fra) · 2, we need (N_int + N_fra) = 75.625.
    - Set Nint = 75 (derived as 4·15 + 2 + 13).
    - Set Nfra = 0.625 (derived as 0.5 + 0.125).
    - Verification: N_div = [(4·15 + 2 + 13) + (0.5 + 0.125)] ·2 = 151.25.

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6. I²C Programming & Control Registers

The programmable features of the R860 are accessible through an I²C-compatible serial interface. Bi-directional data transfer is supported via the serial clock (SCL) and serial data (SDA) lines, operating at clock rates from 100 kHz up to 400 kHz.

I²C Data Transfer Process

The I²C control byte consists of a fixed 7-bit slave address and a read/write (R/W) bit. The default slave address is 0011010 (0x**34**). The R/W bit is set to 0 for write operations and 1 for read operations, as shown in Table 6-1.

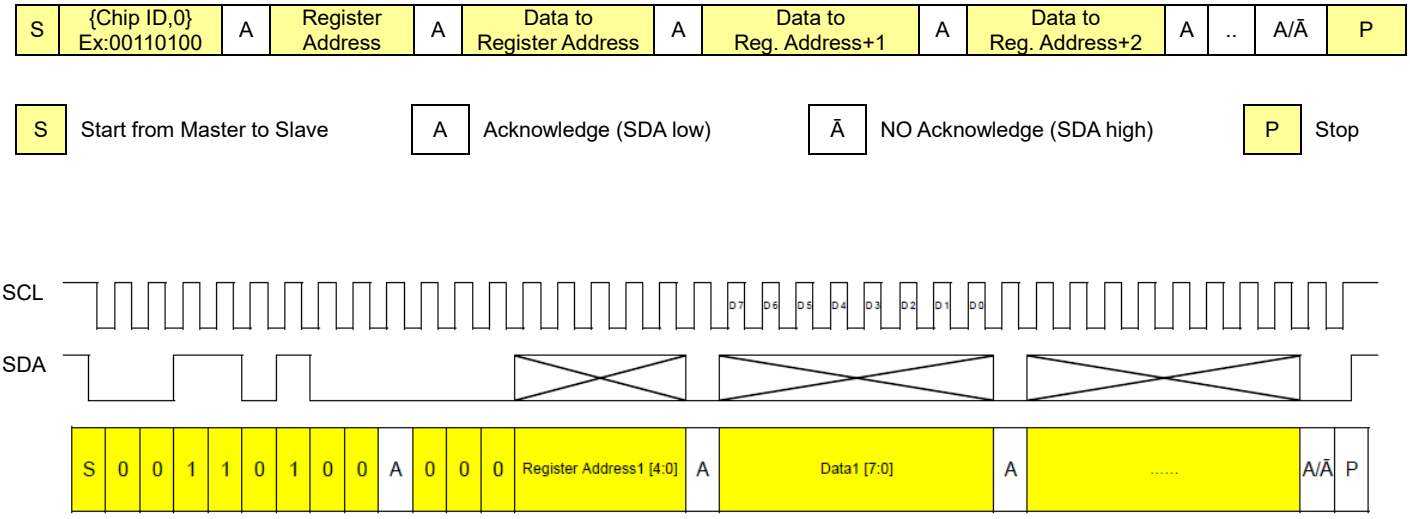
Table 6-1 I²C Write/Read Address

I²C Mode	I²C Address(Binary)R/W								I²C Address (Hex)
	MSB							LSB	
Write Mode	0	0	1	1	0	1	0	0	0x34
Read Mode	0	0	1	1	0	1	0	1	0x35

Write Mode

When the slave address matches the I²C device ID and the R/W bit is set to 0, the I²C interface interprets the next byte as the first register address. All subsequent bytes are treated as register data (page write mode). The first five registers (R0~R4 in Table 6-2) are reserved for internal use and cannot be accessed via I²C write commands.

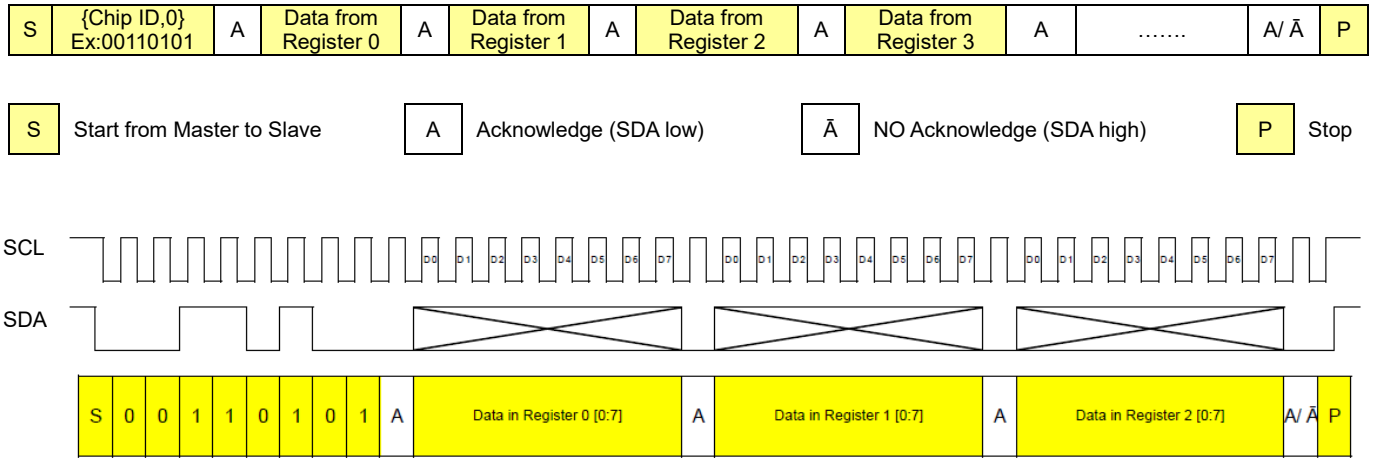
Figure 6-1 Typical Write Sequence (page write I²C process)



Read Mode

When the slave address matches the I²C device ID and the R/W bit is set to 1, data transfer starts immediately after the “ACK” (SDA low). Data is read sequentially from register 0 to the last register until a “P” (STOP) condition occurs. Data is transmitted LSB first, and register 0 contains a fixed value of 0x96, serving as a reference checkpoint for read mode.

Figure 6-2 Typical Read Sequence



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Control Registers

The R860 includes 32 programmable registers for configuring and controlling key functions.

Table 6-2 Register Matrix

Register Address	Name	Read/ Write	B7	B6	B5	B4	B3	B2	B1	B0
0x00	R0	R	1	0	0	1	0	1	1	0
0x01	R1	R	-	-	-	-	-	-	-	-
0x02	R2	R	0	VCO_INDICATOR[6:0] – reserved for internal use only						
0x03	R3	R	RF_INDICATOR [7:0] – reserved for internal use only							
0x04	R4	R	-	-	-	-	-	-	-	-
0x05	R5	R/W	PWD_LT	0	PWD_LNA1	LNA_GAIN_MODE	LNA_GAIN[3:0]			
0x06	R6	R/W	PWD_PDET1	PWD_PDET3	FILT_3DB	1	0	PW_LNA[2:0]		
0x07	R7	R/W	0	PWD_MIX	PW0_MIX	MIXGAIN_MODE	MIX_GAIN[3:0]			
0x08	R8	R/W	PWD_AMP	PW0_AMP	IMR_G[5:0]					
0x09	R9	R/W	PWD_IFFILT	PW1_IFFILT	IMR_P[5:0]					
0x0A	R10	R/W	PWD_FILT	PW_FILT		1	FILT_CODE[3:0]			
0x0B	R11	R/W	0	FILT_BW[1:0]		0	HPF[3:0]			
0x0C	R12	R/W	1	PWD_VGA	1	VGA_MODE	VGA_CODE[3:0]			
0x0D	R13	R/W	LAN_VTHH[4:0]				LNA_VTHL[3:0]			
0x0E	R14	R/W	MIX_VTH_H[3:0]				MIX_VTH_L[3:0]			
0x0F	R15	R/W	0	0	1	CLK_OUT_ENB	1	0	CLK_AGC_ENB	0
0x10	R16	R/W	SEL_DIV[2:0]			REFDIV	0	1	CAPX[1:0]	
0x11	R17	R/W	PW_LDO_A[1:0]		0	0	0	0	1	1
0x12	R18	R/W	1	0	0	0	PW_SDM	0	0	0
0x13	R19	R/W	0	0	0	0	0	0	0	0
0x14	R20	R/W	S_I2C[1:0]		N_I2C[5:0]					
0x15	R21	R/W	SDM_IN[7:0]							
0x16	R22	R/W	SDM_IN[15:8]							
0x17	R23	R/W	PW_LDO_D[1:0]		1	1	OPEN_D	1	0	0
0x18	R24	R/W	0	1	-	-	-	-	-	-
0x19	R25	R/W	PWD_RFFILT	0	0	SW_AGC	1	1	-	-
0x1A	R26	R/W	RFMUX[1:0]		1	0	PLL_AUTO_CLK[1:0]		RFFILT{1:0]	
0x1B	R27	R/W	TF_NCH[3:0]				TF_LP[3:0]			
0x1C	R28	R/W	PDET2_GAIN[3:0]				0	1	-	0
0x1D	R29	R/W	1	1	PDET1_GAIN[2:0]		PDET3_GAIN[2:0]			
0x1E	R30	R/W	0	FILTER_EXT	PDET_CLK[4:0]					
0x1F	R31	R/W	1	1	0	0	0	0	-	-

Table 6-3 Control Register Definitions

Register	R/W	Bitmap	Symbol	Description
R5 0x05	R/W	[7]	PWD_LT	Loop-through on/off 0: on 1: off
	R/W	[5]	PWD_LNA1	LNA 1 power control 0: on 1: off
	R/W	[4]	LNA_GAIN_MODE	LNA gain mode switch 0: auto 1: manual
	R/W	[3:0]	LNA_GAIN[3:0]	LNA manual gain control 1111b: maximum gain ⋮ 0000b: minimum gain
R6 0x06	R/W	[7]	PWD_PDET1	Power detector 1 on/off 0: on 1: off
	R/W	[6]	PWD_PDET3	Power detector 3 on/off 0: off 1: on
	R/W	[5]	FILT_3DB	Filter gain 3dB 0: 0dB 1: +3dB
	R/W	[2:0]	PW_LNA[2:0]	LNA power control 000b: maximum ⋮ 111b: minimum
R7 0x07	R/W	[6]	PWD_MIX	Mixer power 0: off 1: on
	R/W	[5]	PW0_MIX	Mixer current control 0: maximum current 1: normal current
	R/W	[4]	MIXGAIN_MODE	Mixer gain mode 0: manual mode 1: auto mode
	R/W	[3:0]	MIX_GAIN[3:0]	Mixer manual gain control 0000b: minimum ⋮ 1111b: maximum
R8 0x08	R/W	[7]	PWD_AMP	Mixer buffer power on/off 0: off 1: on
	R/W	[6]	PW0_AMP	Mixer buffer current setting 0: high current 1: low current

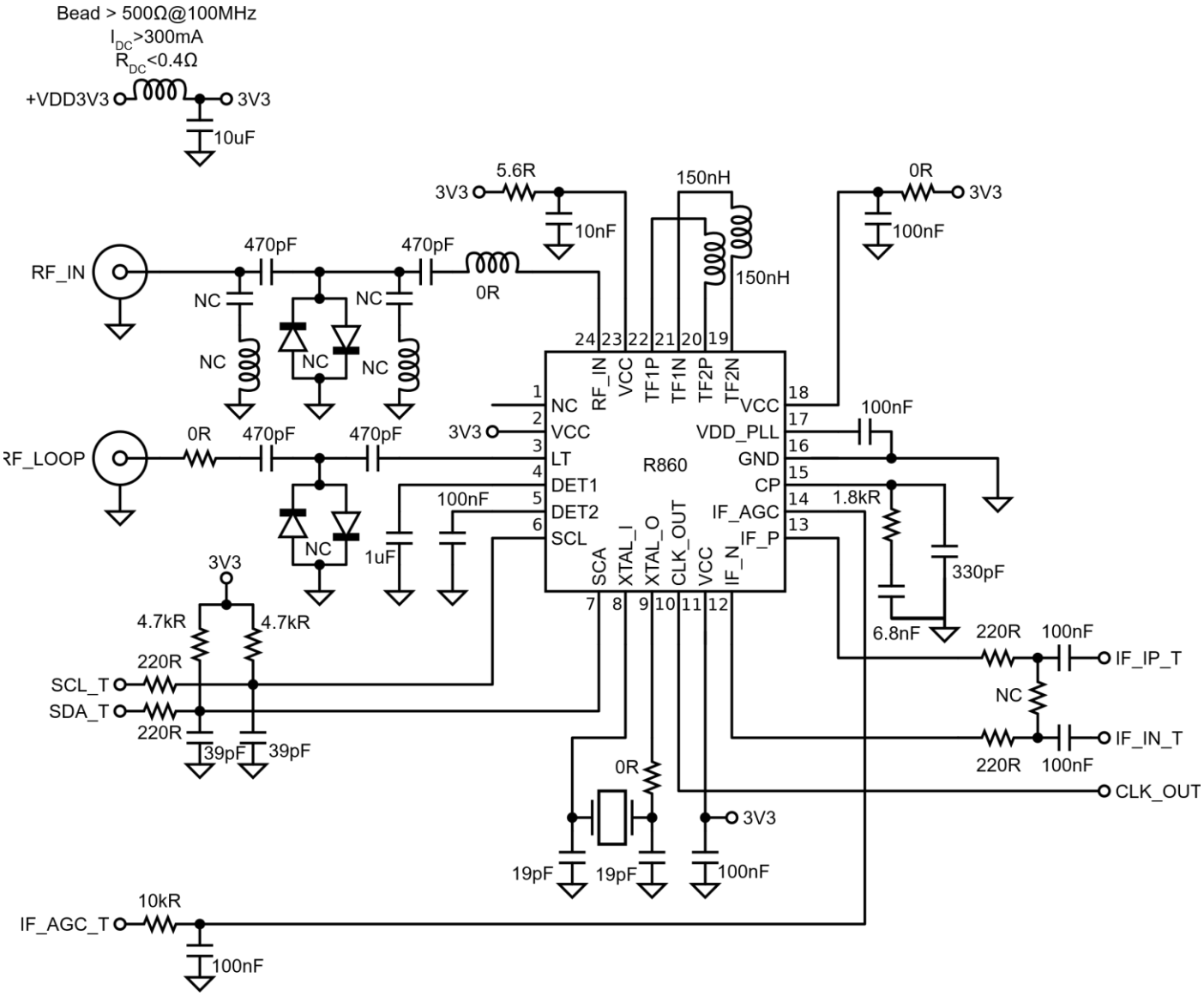
	R/W	[5:0]	IMR_G[5:0]	Image Gain Adjustment 00000b: minimum ⋮ 11111b: maximum
R9 0x09	R/W	[7]	PWD_IFFILT	IF Filter power on/off 0: filter on 1: off
	R/W	[6]	PW1_IFFILT	IF Filter current 0: high current 1: low current
	R/W	[5:0]	IMR_P[5:0]	Image Phase Adjustment 00000b: minimum ⋮ 11111b: maximum
R10 0x0A	R/W	[7]	PWD_FILT	Filter power on/off 0: channel filter off 1: on
	R/W	[6:5]	PW_FILT[1:0]	Filter power control 00b: highest power ⋮ 11b: lowest power
	R/W	[3:0]	FILT_CODE[3:0]	Low pass Filter bandwidth manual fine tune 0000b:widest ⋮ 1111b: narrowest
R11 0x0B	R/W	[6:5]	FILT_BW	Low pass Filter bandwidth manual coarse tune 00b: wide 10b or 01b: Middle 11b: narrow
	R/W	[3:0]	HPF[3:0]	High pass filter corner control 0000b: 5MHz 0001b: 4MHz 0010b: -12dB at 2.25MHz 0011b: -8dB at 2.25MHz 0100b: -4dB at 2.25MHz 0101b: -12dB at 1.75MHz 0110b: -8dB at 1.75MHz 0111b: -4dB at 1.75MHz 1000b: -12dB at 1.25MHz 1001b: -8dB at 1.25MHz 1010b: -4dB at 1.25MHz 1011b: 1MHz 1100b: 0.8MHz 1101b: 0.7MHz 1110b: 0.6MHz 1111b: 0.5MHz
R12 0x0C	R/W	[6]	PWD_VGA	VGA power control 0: VGA power off 1: VGA power on
	R/W	[4]	VGA_MODE	VGA GAIN manual / pin selector 1: IF VGA gain controlled by voltage at IF_AGC pin 0: IF VGA gain controlled by VGA_CODE[3:0]
	R/W	[3:0]	VGA_CODE[3:0]	IF VGA manual gain control (3.5dB/step) 0000b: -12.0 dB ⋮ 1111b: +40.5 dB
R13 0x0D	R/W	[7:4]	LNA_VTHH[4:0]	LNA AGC power detector voltage threshold high setting (~0.1 V/step) 1111b: 1.94 V ⋮ 0000b: 0.34 V

	R/W	[3:0]	LNA_VTHL[3:0]	LNA AGC power detector voltage threshold low setting (~0.1 V/step) 1111b: 1.94 V ⋮ 0000b: 0.34 V
R14 0x0E	R/W	[7:4]	MIX_VTH_H[4:0]	MIXER AGC power detector voltage threshold high setting (~0.1 V/step) 1111b: 1.94 V ⋮ 0000b: 0.34 V
	R/W	[3:0]	MIX_VTH_L[3:0]	MIXER AGC power detector voltage threshold low setting (~0.1 V/step) 1111b: 1.94 V ⋮ 0000b: 0.34 V
R15 0x0F	R/W	[4]	CLK_OUT_ENB	Clock out control 0: clock output on 1: off
	R/W	[1]	CLK_AGC_ENB	AGC clock control 0: internal AGC clock on 1: off
R16 0x10	R/W	[7:5]	SEL_DIV[2:0]	PLL to Mixer divider control 000b: mixer in = vco out /2 001b: mixer in = vco out / 4 010b: mixer in = vco out / 8 011b: mixer in = vco out
	R/W	[4]	REFDIV	PLL Reference frequency Divider 0: f_{ref}=xtal_freq 1: f_{ref}=xta_freq / 2 (for Xtal >24MHz)
	R/W	[1:0]	CAPX[1:0]	Internal xtal capacitor setting 00b: no cap ; 01b: 10pF 10b: 20pF ; 11b: 30pF
R17 0x11	R/W	[7:6]	PW_LDO_A[1:0]	PLL analog low drop-out regulator switch 00b: off 01b: 2.1V 10b: 2.0V 11b: 1.9V
R20 0x14	R/W	[7:6]	S_I2C[1:0]	PLL integer divider number input S_{i2c} $N_{int}=4 \cdot N_{i2c}+S_{i2c}+13$ PLL divider number $N_{div} = (N_{int} + N_{fra}) \cdot 2$
	R/W	[5:0]	N_I2C[5:0]	PLL integer divider number input N_{i2c}
R21 0x15	R/W	[7:0]	SDM_IN[7:0]	PLL fractional divider number input SDM[15:0] $N_{fra}= SDM\_IN[15] \cdot 2^{-1} + SDM\_IN[14] \cdot 2^{-2} + \cdots + SDM\_IN[1] \cdot 2^{-15} + SDM\_IN[0] \cdot 2^{-16}$
R22 0x16	R/W	[7:0]	SDM_IN[15:8]	
	R/W	[7:6]	PW_LDO_D[1:0]	low drop-out regulator for PLL digital supply current 00b: 1.8V,8mA 01b: 1.8V,4mA 10b: 2.0V,8mA 11b: off

R23 0x17	R/W	[3]	OPEN_D	Open drain 0: High-Z 1: Low-Z
R25 0x19	R/W	[7]	PWD_RFFILT	RF Filter power 0: off 1: on
	R/W	[4]	SW_AGC	Switch AGC_pin 0: AGC=AGC_in 1: AGC=AGC_in2
R26 0x1A	R/W	[7:6]	RFMUX[1:0]	Tracking Filter switch 00b: on 01b: bypass
	R/W	[3:2]	PLL_AUTO_CLK[1:0]	PLL auto-tune clock rate 00b: 128 kHz 01b: 32 kHz 10b: 8 kHz
	R/W	[1:0]	RFFILT[1:0]	RF FILTER band selection 00b: high band 01b: middle band 10b: low band
R27 0x1B	R/W	[7:4]	TF_NCH[3:0]	0000b: highest corner for Notch Filter ⋮ 1111b: lowest corner for Notch Filter
	R/W	[3:0]	TF_LP[3:0]	0000b: highest corner for Low Pass Filter ⋮ 1111b: lowest corner for Low Pass Filter
R28 0x1C	R/W	[7:4]	PDET2_TOP[3:0]	Mixer Power detector TOP (take-over point) control 0000b: Highest ⋮ 1111b: Lowest
R29 0x1D	R/W	[5:3]	PDET1_GAIN[2:0]	LNA wideband Power detector TOP (take-over point) control (after LNA, before mixer) 000b: Highest ⋮ 111b: Lowest
	R/W	[2:0]	PDET3_GAIN[2:0]	LNA narrowband Power detector TOP(take-over point) control (after mixer) 000b: Lowest ⋮ 111b: Highest
R30 0x1E	R/W	[6]	FILTER_EXT	Filter extension for weak signal condition 0: Disable 1: Enable
	R/W	[5:0]	PDET_CLK[5:0]	Power detector timing control 111111b: max ⋮ 000000b: min

7. Example schematic

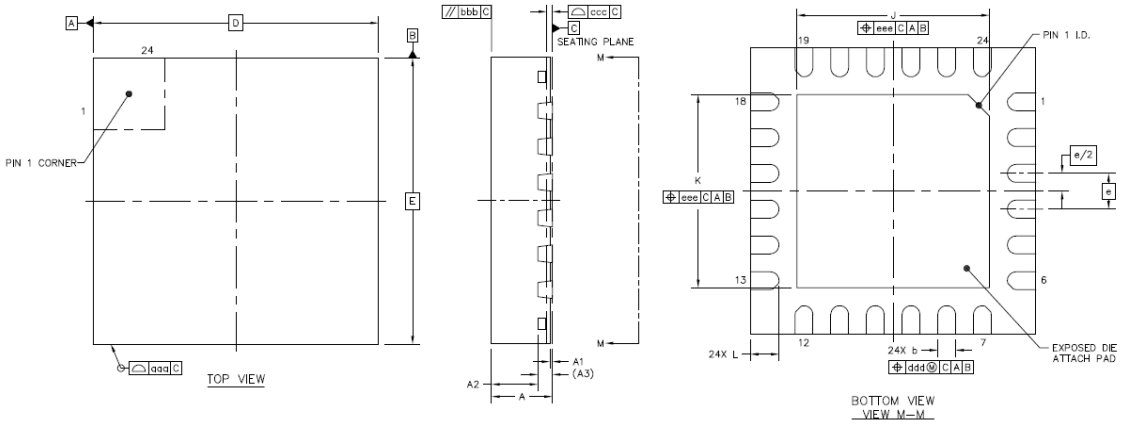
The following figure shows the R860 reference schematic for SDR applications. For detailed design and layout information, refer to the document **"Application Note and Layout Guide – Terrestrial Tuner."**



8. Package Dimensions & Outline

The R860 is offered in a lead-free 4 × 4 mm, 24-pin Quad Flat No-Lead (QFN) package.

Table 8-1 QFN-24 Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A2	---	0.65	---
A3	0.203 REF.		
b	0.20	0.25	0.30
D	4.00 BSC		
D2	2.60	2.70	2.80
E	4.00 BSC		
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
e	0.50 BSC		
Package edge Tolerance(aaa)		0.1	-
MOLD flatness (bbb)		0.1	
COPLANARITY (ccc)		0.08	
LEAD OFFSET(ddd)		0.1	
EXPOSED PAD OFFSET(eee)		0.1	

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Note: Before soldering to system board, the R860 must be baked at 125^{o}C for more than 8 hours to eliminate moisture contamination.

9. Package Markings

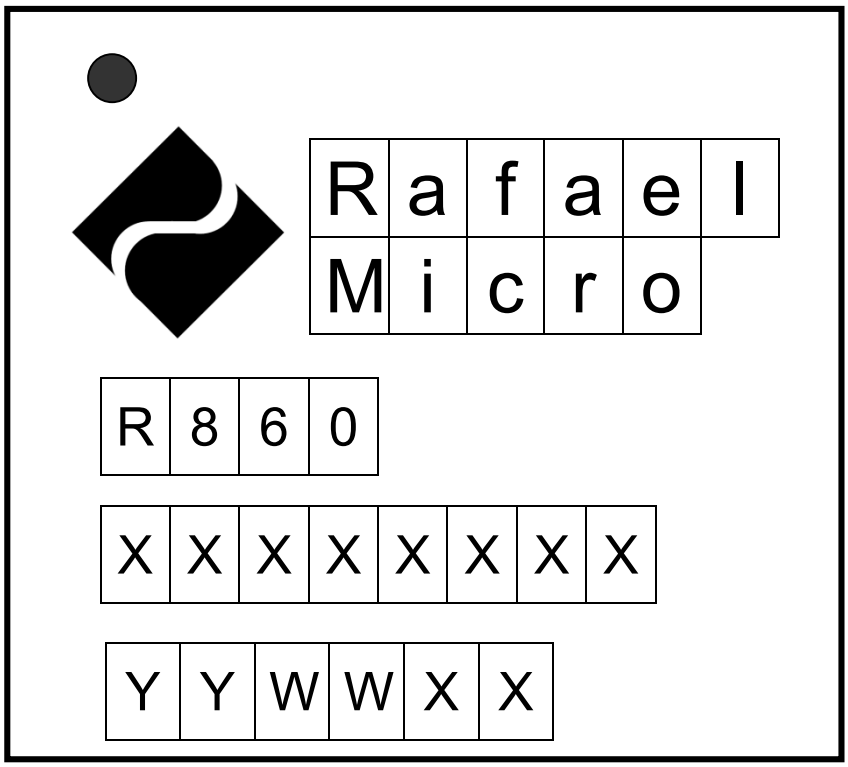


Table 9-1 QFN-24 Package Markings

Marking Method	Laser	
Font Size:	Logo: 3.1mm x 1.3mm Device Number: 0.45mm x 0.3mm MFG Code& Date Code: 0.45mm x 0.3mm Spacing: 0.15mmx0.05mm	
Line 1 Marking	Circle=0.3 mm diameter (Top-left justified)	Pin 1 identifier
Line 2 Marking	Rafael Micro logo	Rafael Micro
Line 3 Marking	Device Number	R860
Line 4 Marking	XXXXXXXX = Manufacturing Code	Manufacturing Code from the Purchase Order to the Packaging & Test Sub-contractor. Manufacturing code varies according to Purchase Order.
Line 5 Marking	YYWWXX	Assigned by the Packaging & Test Sub-contractor.
	YY = Year; WW = Work Week	Corresponds to the year & work week of the mold date.
	XX= Control Code	Rafael Micro internal control code (manufacturing).

10. Contact Information

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11. Revision History

Revision	Description	Owner	Date
1.0	First official release	Mitsui Chen	2020/06/29
1.1	Update tuning range for consistency & modify legal notice (last page)	Mitsui Chen	2020/08/11
1.2	Correct the description of clock_output signal control in Section 4	Mitsui Chen	2020/10/28
1.3	Correct the topic of data sheet	Mitsui Chen	2021/08/13
1.4	Correct the frequency range	Kare Chen	2024/11/28
1.5	Reorganize and enhance the document by adding sections such as **"Performance Characteristics"** and **"Theory of Operation."**	Benjamin Chen	2025/11/5
1.6	Update Table 2.2 AC parameter and 4. Performance Characteristics.	Benjamin Chen	2026/3/10